Katherine Mohr

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Interests

Compilers, Performance Engineering, Networking, Computer Architecture

Education

Stanford University *Stanford, CA*
PhD in Computer Science *Sept 2025 - Jun 2030 (expected)*

Massachusetts Institute of Technology *Cambridge, MA*
Master of Engineering & Bachelor of Science in Electrical Engineering and Computer Science *Sept 2019 - Aug 2024*

- **GPA:** 5.0/5.0
- **Teaching:** Programming Language Design, Dynamic Computer Language Eng, Graphics, Differential Equations
- **Awards:** 2023 SuperUROP Outstanding Research Award

Experience

Five Rings *New York, NY*
Software Developer *Aug 2024 - Sept 2025*

- Operated as a C++ generalist in a high-performance trading environment, building internal developer tooling, delivering trader-requested features, and refactoring latency-sensitive systems to enhance speed and efficiency across the codebase

Compilers at MIT (COMMIT) Group *Advisor: Saman Amarasinghe*
Graduate Researcher *Sept 2023 - Aug 2024*

- Developed a new technique to seamlessly migrate packet processing from an optimized kernel module to an unoptimized user application via on-stack replacement, to improve the correctness and performance of prior work

Undergraduate Researcher (SuperUROP) *Sept 2022 - June 2023*

- Worked on LakePlacid, a system of compilers for optimizing networking applications with profile-guided optimization
- Designed and implemented a new toolchain for applying arbitrary compiler passes to some given source code
- Proposed and evaluated an improved method for identifying the most important application logic based on profiling data of varied networking workloads

Adobe *San Francisco Bay Area*
Software Developer Intern *June 2023 - Aug 2023*

- Implemented and tested different tactics for managing competing threads and prioritizing renders to improve efficiency and make background rendering less noticeable by Premiere Pro users

Computer Scientist Intern (C++) *May 2022 - Aug 2022*

- Built an end-to-end GPU inference pipeline to prevent slowdowns due to extraneous copies between the CPU and GPU

Visual Computing Languages and Systems (VCLS) Group *Advisor: Jonathan Ragan-Kelley*
Undergraduate Researcher (UROP) *Sept 2021 - June 2022*

- Developed a new tool for generating efficient pattern-matching code for Halide's term rewriting system (TRS)
- Optimized the new TRS with constant folding improvements, pointer reuse analysis, and jump tables

LinkedIn *San Francisco, CA*
Software Engineer Intern *June 2021 - Aug 2021*

- Restructured plugin schemas and refactored code to allow messaging plugins to securely access private fields
- Reorganized messaging delivery logic to improve maintainability and make the codebase fully use case agnostic

UnifyID (acquired by Prove) *Redwood City, CA*
Software Engineering Intern *Aug 2020 - Jan 2021*

- Created a pipeline to train and analyze gait models for individual users, implemented scripts for validating and ingesting external datasets, and improved methods for optimizing score policy configurations
- Designed and developed an initial automated performance regression pipeline to easily validate and track the accuracy and speed of our machine learning models after each version change